

# IMPLEMENTATION OF MULTILEVEL INVERTER USING SPACE VECTOR PULSE WIDTH MODULATION

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**ABSTRACT:** The objective of the present work is to obtain less distorted, higher power AC output from a 3-phase, 3-level, diode-clamped inverter using Space Vector Pulse Width Modulation Technique as a control strategy. The multilevel inverters with space vector pulse width modulation technique have established their importance in high performance, high power industrial application because of their several advantages over ordinary single level inverter in terms of its lower dv/dt stress, lower rating component and higher efficiency. In our work, a three-phase, three-level diode clamped inverter has been designed and implemented using MOSFET as switches. By formulating a specific switching pattern, we have created three levels in line-line voltage and five levels in phase voltage by using four MOSFETs as switches in one leg of inverter. For pulse generation, we are using Space Vector Pulse Width Modulation (SVPWM) technique by comparing a carrier signal with a reference signal. This technique has many industrial applications like speed control of induction motor. This modulation technique can reduce the Total Harmonic Distortion (THD) and improve voltage magnitude across load. All output results for resistive loads and inductive loads (Motor) along with their FFT analysis have been discussed in this paper.

**KEYWORDS:** Multilevel Inverter. THD. Space Vector PWM. MOSFET

## 1.0 INTRODUCTION

In the recent times, Inverters have found its way into many fields of Power electronics applications and Power System research work. The multilevel inverter is the class of inverter in which a stepped AC output waveform is generated from the combination of many switches so as to minimize dv/dt and THD. Those steps being supplied from different DC levels made by series connected batteries or capacitors. By increasing number of levels, the output voltage waveform will have more steps, producing a very fine stair-case and approaching very closely to a pure sinusoidal waveform. Hence this technique offers better efficiency at the high power end using low voltage rating components without the problems of high dv/dt and other associated issues.

## 2.0 CONCEPT OF MULTILEVEL INVERTER

The conventional inverter can generate only two different levels of voltages for the load. These two voltage levels are switched with the PWM. The multilevel inverter (MLI) do not depends on two levels of voltage to create AC signal. Instead several voltage levels are added to one another to create a smooth step AC waveform. That smooth waveform has many advantages such that reduction in electromagnetic compatibility (EMC), smaller common mode (CM) voltage and generation of high voltage using low voltage rating components.<sup>[1]</sup> The only disadvantage of this technique is that by increasing the levels, the number of switches will increase and the switching combination will become complex and control will become complicated and expensive. Its various applications are in Renewable DC source utilization, Uninterruptible Power Supplies (UPS), Power Transmission through high voltage DC (HVDC), Variable frequency drives and electrical vehicle drives.<sup>[2]</sup>

### 2.1 DIODE CLAMPED INVERTER

Multilevel inverter (MLI) has many implementation techniques such that Cascaded Multilevel Inverter, Diode clamped Multilevel Inverter and Flying capacitor inverter. In our work, we have implemented Diode Clamped inverter. This inverter provides multiple voltage levels through connection of a series of capacitors. Figure 1 is showing the

topology of three-level diode clamped inverter. By following the convention, this topology can be extended at any level by increasing the number of capacitors and diodes. In this topology, the clamping diodes are essential to provide the path for reverse current. Although this structure is more complicated to the conventional two-level inverter but it is straight forward and symmetric. A common DC bus is divided by an even number of capacitors depending upon the number of levels in the inverters. A neutral point will be in the middle of the capacitor bank. Clamping diodes will be used to connect the load to the neutral point.

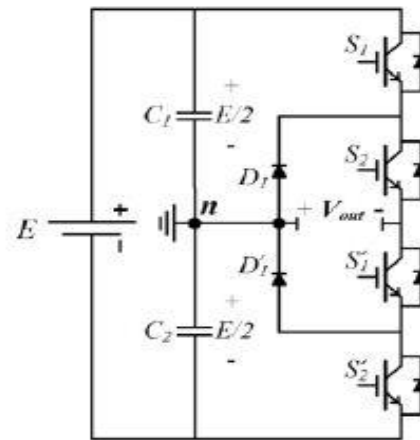


Fig 1: one leg of three-level diode clamped inverter

The advantages of this topology are its high efficiency, its low cost and lesser number of components.<sup>[3]</sup> In this topology, all the phases share a common DC sources which minimizes the issue of short circuit of isolated sources. Due to symmetry, it can be implemented as cascaded configuration and can be extended to any level. This topology has a disadvantage of the real power flow because of non-uniform or over-charging of capacitors.

### 2.2 SIMULATION

The first step of the project was complete simulation of the inverter. We have simulated the whole project on Simulink

MATLAB. The hardware design was simulated using MOSFET switches and the complete simulated 3-phase hardware is shown in the fig 2.<sup>[4]</sup>

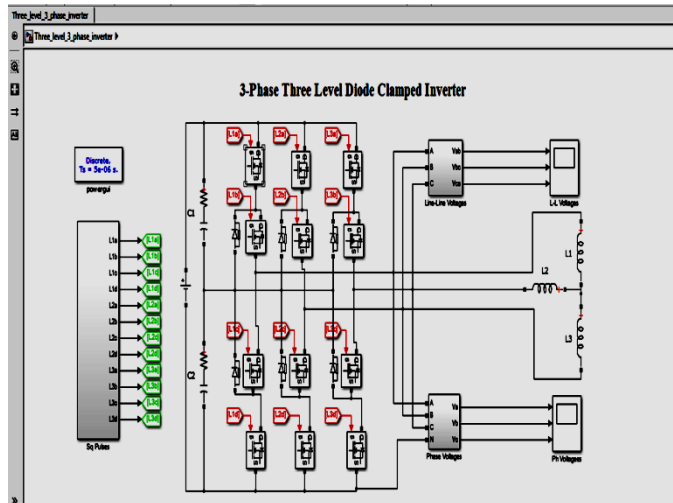


Fig 2: Hardware simulation of 3-level, 3-phase diode clamped inverter

For software implementation in MATLAB, we have used the basic technique of comparison between sinusoidal reference signal and triangular pulse for each level. That comparison gave the SVPWM pulses which are provided to the hardware design. The block diagram of implementation of SVPWM pulses is given in fig 3.

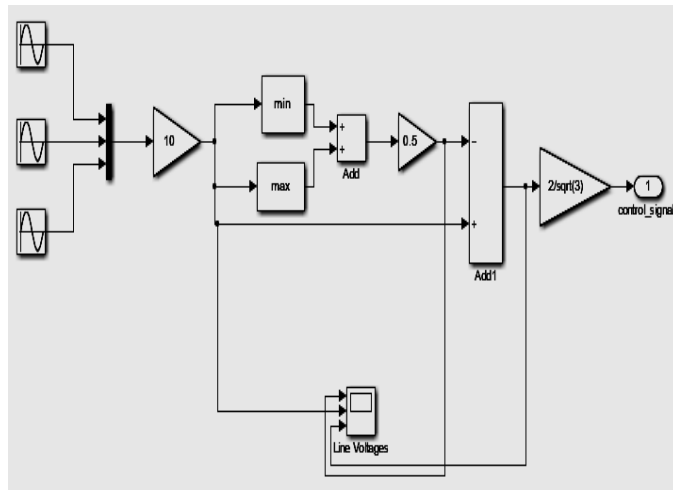


Fig 3: Space Vector PWM implementation in MATLAB

These pulses when provided to the system which gave the desired output waveform which is shown in fig 4.

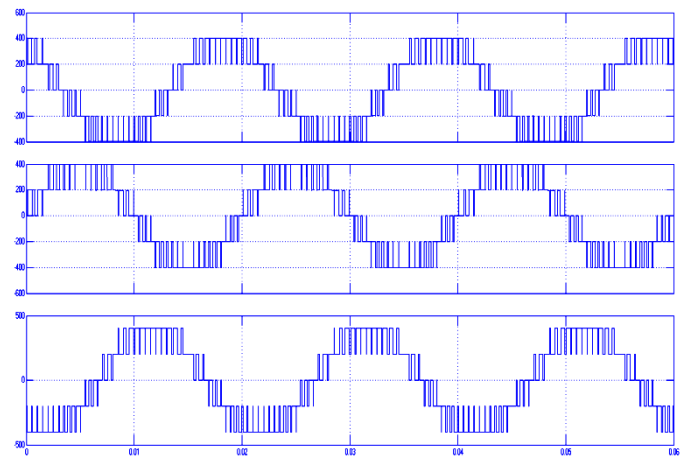


Fig 4: Simulated output waveform of diode clamped inverter (Line-to-line voltage)

### 3.0 SYSTEM IMPLEMENTATION

The implementation of the inverter consists of two phases, i.e hardware implementation and software implementation.

#### 3.1 HARDWARE IMPLEMENTATION

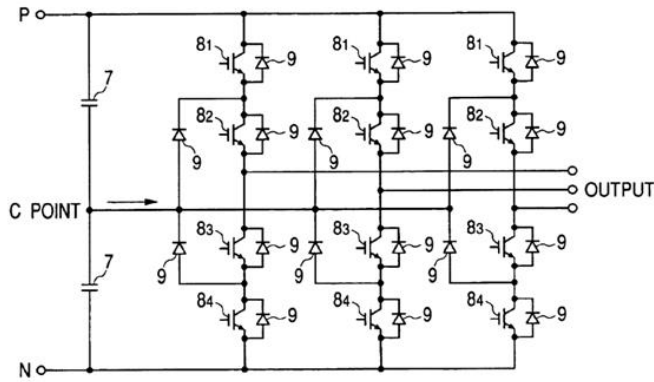
In general, for three-phase, m-level diode clamped inverter, we are required a total of  $2(m-1)$  number of switches per phase,  $(m-1)(m-2)$  clamping diode per phase,  $(m-1)$  DC bus capacitors, thus required components of three-phase, three-level inverter, we were needed a total of 6 clamping diode, 12 semi-conductor switches and 2 DC Bus capacitors. The complete circuit diagram of three-phase, three-level inverter is given in fig 5.

The components were chosen according to our requirements or feasibility. Our aim was to generate high power inverter using low cost, low power components. The main requirements of our actual hardware are given below:

- ⇒ We want to drive a motor of 1hp with minimum vibrations and minimum total harmonic distortion (THD). The rated voltage of the motor is 230V and maximum output current drawn by it is almost 5A.
- ⇒ The switching frequency of the carrier wave for SPWM is at-least 4KHz. So we need switching devices and clamping diodes which can switch at this frequency with lowest switching losses.

Thus by consulting some literature and keeping in view our goal, we selected these components for our inverter.

- ⇒ IRF450 Semiconductor (MOSFET) switches.
- ⇒ UF4007 Ultra-fast clamping diodes.
- ⇒ Electrolytic capacitors
- ⇒ TLP250 opto-coupler IC for protection of Microcontroller and PWM generation.
- ⇒ STM32F303 Microcontroller for software implementation.



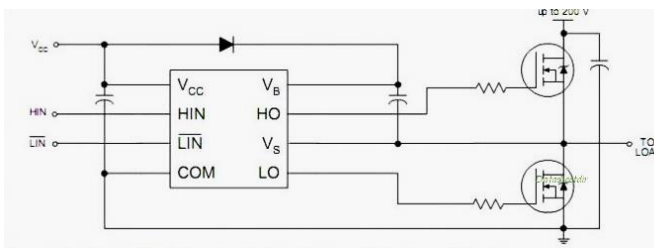
**Fig 5: hardware schematic of three-phase three-level diode clamped inverter**

The choice of our components was based on the analysis of their fast switching frequency, Dynamic Low dv/dt stresses due to fast switching, low cost, Ease of paralleling, availability in the market, flexibility, reliability, high efficiency and longer capability.

After selecting the required components, the design was tested on each stage. Initial testing was based on the testing of each leg of inverter and interfaced it with PWM control to verify its output. As we had to control 4 switches per leg and each switch will require a pulse for switching its gate with respect to source. Thus, we are required a total of 4 pulses at gate with respect to 4 different sources. This problem of virtual ground can be solved by two methods:

- ⇒ By using gate driver IC which provided virtual ground at the output with the help of a capacitor
- ⇒ By using isolated supplies using multiple transformers.

We tested both methods one by one. The first methodology was designed using IR 2103 gate driver IC and its design is shown in the figure 6.

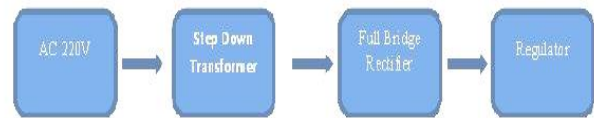


**Fig 6: Gate Driver basic control circuit**

The working of gate driver belongs to the charging and discharging of capacitor which is connected at pin 8 of gate driver IC and load (pin 6). Due to continuous charging and discharging of capacitor with the load, a square wave will be generated at pin 7 and pin 6. Pin 6 will act as virtual ground for the control circuit. We tried different topologies for controlling 4 switches with either 4 Date drivers or with 2

Gate driver ICs. But they did not work for the multi-level inverter due to the reason that there is no discharging path available for each capacitor. To have a virtual ground at the output of gate driver, there must be charging/discharging path for each capacitor inside the circuit. In two-level inverter, that path is provided by the load but for three-level inverter, there are 4 separate sources of 4 MOSFETs and load will be connected to only one node. Hence, the gate driver connected with source of switch S1 and switch S3 will not have any discharging path as there is no resistance provided at these nodes. So it will not provide virtual ground to the circuit. Due to this issue, gate driver IC does not work after two-level inverter. To provide a virtual ground, a discharging/charging has to be supplied to each capacitor of Gate Driver control circuit which is not possible in multi-level inverter.

After the poor performance of gate driver control circuit, we switched to the isolated DC supplies using transformers. We used step down transformers, rectified the output of the transformer and regulated the DC output with regulator IC 7815. The topology is shown in a block diagram in fig 7. This methodology worked fine and gave the desired result.



**Fig 7: Block Diagram of isolated supplies Implementation**

After the initial testing phase, we concluded that switches can be controlled using isolated power supplies. So the next step was to make 12 isolated supplied for 12 MOSFET Switches. So we implemented our control unit with the following parts:

- ⇒ Transformer Units: We used PCB mounted 1 primary, 2 secondary 220V/12V transformers. As we require a total of 12 supplies for 12 switches (4 per leg), so we design 6 transformers.
- ⇒ Rectifier Unit: The output of these step-down transformers is rectified using rectifier unit. It consists of 12 bridge rectifiers which are giving us 12 pulsating DC output voltages.
- ⇒ Regulation Unit: The output of rectifier unit is fed to the series of regulators which are regulating the pulsating DC voltage to regulate +15V isolated voltages which are fed to the inverter for switching action.

The complete control unit schematic on Proteus ISIS is shown in the fig 8 below.

The other part was our actual hardware which was made up of TLP250 Opto-couplers and IRF450 MOSFET switches. The complete hardware diagram is shown in figure 9.

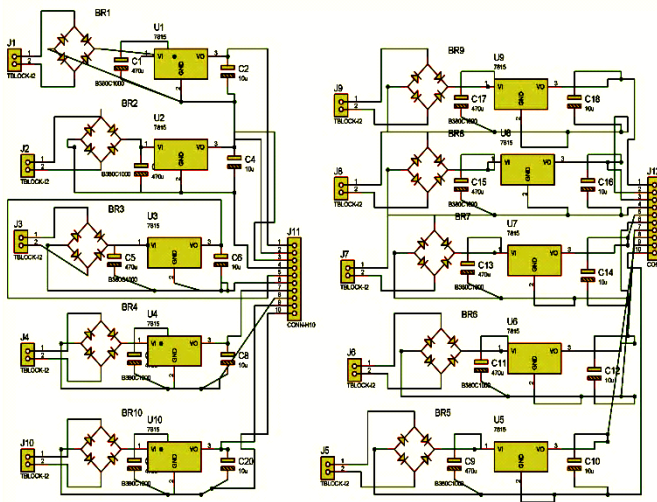


Fig 8: Complete control unit Schematic

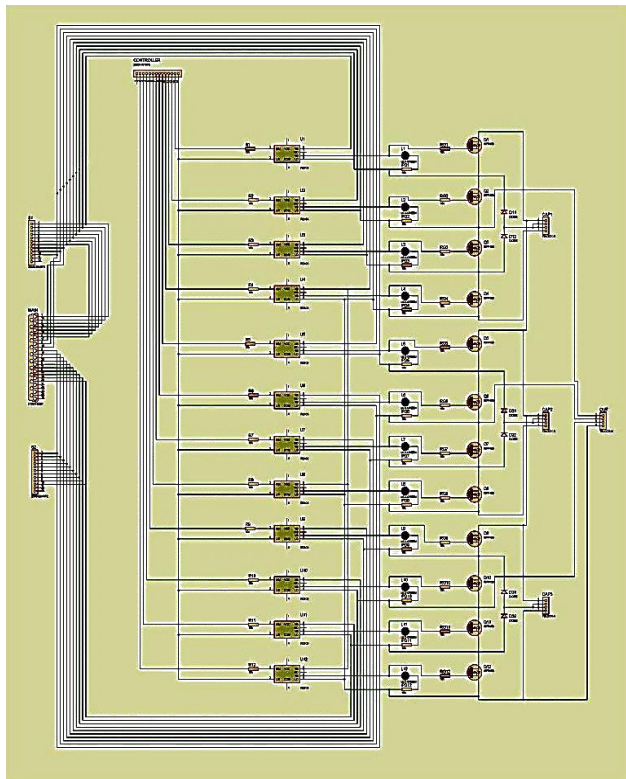


Fig 9: Complete Switching unit Schematic

**3.2 SOFTWARE IMPLEMENTATION**

Space Vector Pulse Width Modulation (SVM) technique was used for switching the semi-conductor switches to generate less distorted sinusoidal waveform. Space Vector Modulation (SVM) is a technique to control the power switches in an appropriate sequence so that the switching loss reduces and efficiency increases. Output voltage and input current can be controlled by Space vector Pulse Width Modulation (SVPWM). We can choose both input current and output voltage using switching vector to control the inverter which has provided more flexibility in control. It can yield useful advantage under unbalanced conditions. The advantages of space vector modulation over other techniques

are given below:

- ⇒ SVPWM also has good utilization of the DC link voltage, low current ripple and relative easy hardware implementation.
- ⇒ Compared to the SPWM, the SVPWM has a 15% higher magnitude of the output voltage.
- ⇒ SVM generates less harmonic distortion in output voltage or current as compared to SPWM.
- ⇒ SVM provides more efficient use of supply voltage as compared to all other modulation techniques. This feature and better efficiency makes this technique suitable for high voltage high power applications, like renewable power generation

In this method, the three phase variables are expressed in space vectors. It generates the appropriate gate drive waveform for each PWM cycle. The whole circuit is assumed as one single unit and can combine different number of switching states. That switching states depend on the number of levels. The SVPWM provides unique switching time calculations for each of these states. Switching pattern for higher levels can also be developed by using this technique easily. All kinds of multilevel inverters (cascaded, capacitor clamped, diode clamped) can be controlled with this modulation strategy. The three vectors that form one triangle will provide duty cycle time for each, giving the desired voltage vector  $V_{ref}$ .

The general SVM vector chart for three-level inverter is shown in the figure 10. The three-phase, three-level inverter can be characterized by  $3^3 = 27$  switching states as indicated in the figure 10 where each phase can have P, N, O state. There are 24 active states while remaining three (PPP, NNN, OOO) are zero states which are the center of hexagon. The area of the whole hexagon can be divided into 6 sectors (I to VI). Each sector will contain four regions (1 to 4). In this way, we can have 24 regions of operation. The command voltage can be expanded from zero to that inscribed in the large hexagon by changing the modulation index.<sup>[5]</sup>

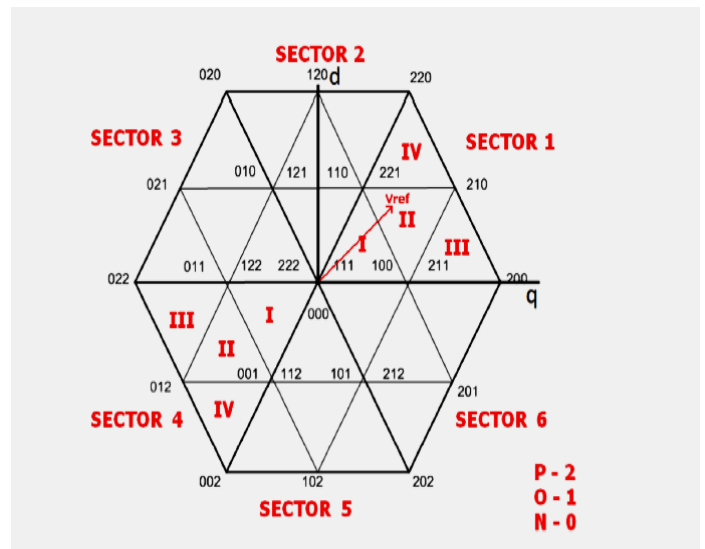


Fig 10: Space Vector Chart

There are many methods to implement space vector modulation. We implemented the open-loop modulation at fixed modulation index of 0.907. We compared the square pulses of switching frequency of 4 KHz with a special reference signal which is made by inspecting all the sectors of space-vector chart. The reference signal for other two phases will be 120 degrees out of phase. Three carrier signals having offset of peak value in between them are compared with the reference signal provide the required pulses for each gate of MOSFET. In this way, we implemented the fixed modulation-index space vector modulation. The reference signal along with the carrier signals are plotted in the figure 11.<sup>[5]</sup>

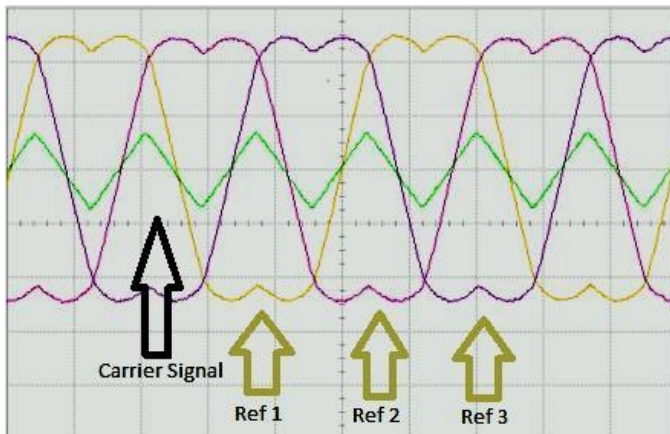


Fig 11: Reference and carrier signal of SVM

**4.0 ANALYSIS AND EVALUATION**

The output waveform of the inverter under the space vector PWM control is shown in the figure 12. It contains 3 levels in line-to-line voltage and 5 levels in phase voltage. The line-to-line voltage waveform along with its frequency transform is shown in the figure 12 and 13 respectively. With the frequency analysis of the output waveform, the performance parameters of the output were calculated. The output waveform contained only 3% THD which was highly desired.



Fig 12: Output Line-to-line voltage over SVM control

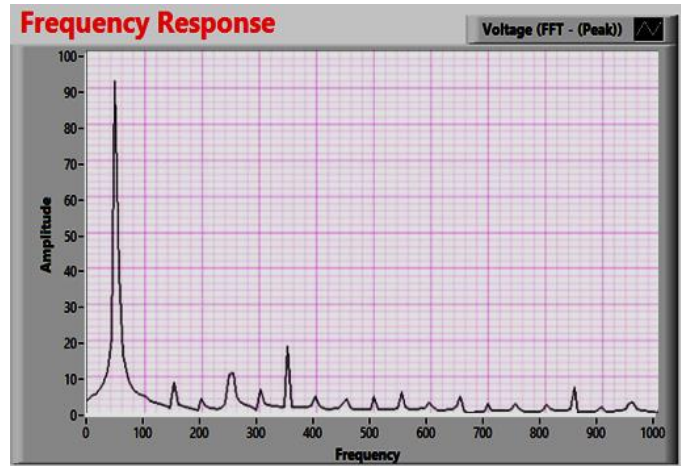


Fig 13: FFT of Output Line-to-line voltage over SVM control

**5.0 CONCLUSION**

As efficiency is becoming increasingly important in power electronics, it is the goal of each and every industry and research laboratory to take up some initiatives to reduce energy crisis and power consumption by inventing new methods to improve efficiency of the product. In that dimension, multilevel inverter is the vital step. This paper described the advantages/disadvantages of multilevel inverter and its applications in industry. It has covered the design requirements and design procedures of the inverter. It has described a detailed hardware testing and its implementation. It also covered implementation of SVPWM for a three-level diode clamped inverter. The popular space vector modulation strategy incorporated with the balancing controller for the DC-link capacitor. In order to provide more details, this paper has offered a detailed approach with designs, verifications and validations using MATLAB / SIMULINK which will be, hopefully, useful for students and researchers.

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